Release 14.7 - xst P.20131013 (nt64)

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--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.08 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.08 secs

--> Reading design: Bryant\_CSM\_8B.prj

TABLE OF CONTENTS

1) Synthesis Options Summary

2) HDL Compilation

3) Design Hierarchy Analysis

4) HDL Analysis

5) HDL Synthesis

5.1) HDL Synthesis Report

6) Advanced HDL Synthesis

6.1) Advanced HDL Synthesis Report

7) Low Level Synthesis

8) Partition Report

9) Final Report

9.1) Device utilization summary

9.2) Partition Resource Summary

9.3) TIMING REPORT

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\* Synthesis Options Summary \*

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---- Source Parameters

Input File Name : "Bryant\_CSM\_8B.prj"

Input Format : mixed

Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "Bryant\_CSM\_8B"

Output Format : NGC

Target Device : xc4vlx100-12-ff1148

---- Source Options

Top Module Name : Bryant\_CSM\_8B

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Mux Style : Auto

Decoder Extraction : YES

Priority Encoder Extraction : Yes

Shift Register Extraction : YES

Logical Shifter Extraction : YES

XOR Collapsing : YES

ROM Style : Auto

Mux Extraction : Yes

Resource Sharing : YES

Asynchronous To Synchronous : NO

Use DSP Block : Auto

Automatic Register Balancing : No

---- Target Options

Add IO Buffers : YES

Global Maximum Fanout : 100000

Add Generic Clock Buffer(BUFG) : 32

Number of Regional Clock Buffers : 48

Register Duplication : YES

Slice Packing : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Auto

Use Synchronous Set : Auto

Use Synchronous Reset : Auto

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed

Optimization Effort : 1

Power Reduction : NO

Keep Hierarchy : No

Netlist Hierarchy : As\_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

DSP48 Utilization Ratio : 100

Verilog 2001 : YES

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

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\* HDL Compilation \*

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WARNING:HDLParsers:3607 - Unit work/Bryant\_CSMSlice is now defined in a different file. It was defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSM\_Components.vhdl", and is now defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

WARNING:HDLParsers:3607 - Unit work/Bryant\_CSMSlice/behv is now defined in a different file. It was defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSM\_Components.vhdl", and is now defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

WARNING:HDLParsers:3607 - Unit work/Bryant\_CSMLastSlice is now defined in a different file. It was defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSM\_Components.vhdl", and is now defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

WARNING:HDLParsers:3607 - Unit work/Bryant\_CSMLastSlice/behv is now defined in a different file. It was defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSM\_Components.vhdl", and is now defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

WARNING:HDLParsers:3607 - Unit work/Bryant\_GenReg is now defined in a different file. It was defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSM\_Components.vhdl", and is now defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

WARNING:HDLParsers:3607 - Unit work/Bryant\_GenReg/reg16bit\_arch is now defined in a different file. It was defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSM\_Components.vhdl", and is now defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

WARNING:HDLParsers:3607 - Unit work/Bryant\_GenRegLast is now defined in a different file. It was defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSM\_Components.vhdl", and is now defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

WARNING:HDLParsers:3607 - Unit work/Bryant\_GenRegLast/reg16bit\_arch is now defined in a different file. It was defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSM\_Components.vhdl", and is now defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

WARNING:HDLParsers:3607 - Unit work/Bryant\_CSMSlice\_2B is now defined in a different file. It was defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSM\_Components.vhdl", and is now defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

WARNING:HDLParsers:3607 - Unit work/Bryant\_CSMSlice\_2B/behv is now defined in a different file. It was defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSM\_Components.vhdl", and is now defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

WARNING:HDLParsers:3607 - Unit work/Bryant\_CSMLastSlice\_2B is now defined in a different file. It was defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSM\_Components.vhdl", and is now defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

WARNING:HDLParsers:3607 - Unit work/Bryant\_CSMLastSlice\_2B/behv is now defined in a different file. It was defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSM\_Components.vhdl", and is now defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

WARNING:HDLParsers:3607 - Unit work/Bryant\_CSMSlice\_4B is now defined in a different file. It was defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSM\_Components.vhdl", and is now defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

WARNING:HDLParsers:3607 - Unit work/Bryant\_CSMSlice\_4B/behv is now defined in a different file. It was defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSM\_Components.vhdl", and is now defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

WARNING:HDLParsers:3607 - Unit work/Bryant\_CSMLastSlice\_4B is now defined in a different file. It was defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSM\_Components.vhdl", and is now defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

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WARNING:HDLParsers:3607 - Unit work/Bryant\_CSMSlice\_6B is now defined in a different file. It was defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSM\_Components.vhdl", and is now defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

WARNING:HDLParsers:3607 - Unit work/Bryant\_CSMSlice\_6B/behv is now defined in a different file. It was defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSM\_Components.vhdl", and is now defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

WARNING:HDLParsers:3607 - Unit work/Bryant\_CSMLastSlice\_6B is now defined in a different file. It was defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSM\_Components.vhdl", and is now defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

WARNING:HDLParsers:3607 - Unit work/Bryant\_CSMLastSlice\_6B/behv is now defined in a different file. It was defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSM\_Components.vhdl", and is now defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

WARNING:HDLParsers:3607 - Unit work/Bryant\_CSMSlice\_8B is now defined in a different file. It was defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSM\_Components.vhdl", and is now defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

WARNING:HDLParsers:3607 - Unit work/Bryant\_CSMSlice\_8B/behv is now defined in a different file. It was defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSM\_Components.vhdl", and is now defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

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WARNING:HDLParsers:3607 - Unit work/Bryant\_CSMLastSlice\_8B/behv is now defined in a different file. It was defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSM\_Components.vhdl", and is now defined in "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

Compiling vhdl file "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl" in Library work.

Architecture behv of Entity bryant\_csmslice is up to date.

Architecture behv of Entity bryant\_csmlastslice is up to date.

Architecture reg16bit\_arch of Entity bryant\_genreg is up to date.

Architecture reg16bit\_arch of Entity bryant\_genreglast is up to date.

Architecture behv of Entity bryant\_csmslice\_2b is up to date.

Architecture behv of Entity bryant\_csmlastslice\_2b is up to date.

Architecture behv of Entity bryant\_csmslice\_4b is up to date.

Architecture behv of Entity bryant\_csmlastslice\_4b is up to date.

Architecture behv of Entity bryant\_csmslice\_6b is up to date.

Architecture behv of Entity bryant\_csmlastslice\_6b is up to date.

Architecture behv of Entity bryant\_csmslice\_8b is up to date.

Architecture behv of Entity bryant\_csmlastslice\_8b is up to date.

Compiling vhdl file "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSM\_8B.vhdl" in Library work.

Entity <Bryant\_CSM\_8B> compiled.

Entity <Bryant\_CSM\_8B> (Architecture <CSM\_8B>) compiled.

=========================================================================

\* Design Hierarchy Analysis \*

=========================================================================

Analyzing hierarchy for entity <Bryant\_CSM\_8B> in library <work> (architecture <CSM\_8B>) with generics.

BITS2 = 2

BITS4 = 4

BITS6 = 6

BITS8 = 8

W = 24

Analyzing hierarchy for entity <Bryant\_CSMSlice\_8B> in library <work> (architecture <behv>) with generics.

BBITS = 8

W = 24

Analyzing hierarchy for entity <Bryant\_GenReg> in library <work> (architecture <reg16bit\_arch>) with generics.

bbits = 16

w = 32

Analyzing hierarchy for entity <Bryant\_CSMSlice\_8B> in library <work> (architecture <behv>) with generics.

BBITS = 8

W = 32

Analyzing hierarchy for entity <Bryant\_GenReg> in library <work> (architecture <reg16bit\_arch>) with generics.

bbits = 32

w = 40

Analyzing hierarchy for entity <Bryant\_CSMLastSlice\_8B> in library <work> (architecture <behv>) with generics.

BBITS = 8

W = 40

Analyzing hierarchy for entity <Bryant\_GenRegLast> in library <work> (architecture <reg16bit\_arch>) with generics.

w = 48

Analyzing hierarchy for entity <Bryant\_CSMSlice> in library <work> (architecture <behv>) with generics.

W = 24

Analyzing hierarchy for entity <Bryant\_CSMSlice> in library <work> (architecture <behv>) with generics.

W = 25

Analyzing hierarchy for entity <Bryant\_CSMSlice> in library <work> (architecture <behv>) with generics.

W = 26

Analyzing hierarchy for entity <Bryant\_CSMSlice> in library <work> (architecture <behv>) with generics.

W = 27

Analyzing hierarchy for entity <Bryant\_CSMSlice> in library <work> (architecture <behv>) with generics.

W = 28

Analyzing hierarchy for entity <Bryant\_CSMSlice> in library <work> (architecture <behv>) with generics.

W = 29

Analyzing hierarchy for entity <Bryant\_CSMSlice> in library <work> (architecture <behv>) with generics.

W = 30

Analyzing hierarchy for entity <Bryant\_CSMSlice> in library <work> (architecture <behv>) with generics.

W = 31

Analyzing hierarchy for entity <Bryant\_CSMSlice> in library <work> (architecture <behv>) with generics.

W = 32

Analyzing hierarchy for entity <Bryant\_CSMSlice> in library <work> (architecture <behv>) with generics.

W = 33

Analyzing hierarchy for entity <Bryant\_CSMSlice> in library <work> (architecture <behv>) with generics.

W = 34

Analyzing hierarchy for entity <Bryant\_CSMSlice> in library <work> (architecture <behv>) with generics.

W = 35

Analyzing hierarchy for entity <Bryant\_CSMSlice> in library <work> (architecture <behv>) with generics.

W = 36

Analyzing hierarchy for entity <Bryant\_CSMSlice> in library <work> (architecture <behv>) with generics.

W = 37

Analyzing hierarchy for entity <Bryant\_CSMSlice> in library <work> (architecture <behv>) with generics.

W = 38

Analyzing hierarchy for entity <Bryant\_CSMSlice> in library <work> (architecture <behv>) with generics.

W = 39

Analyzing hierarchy for entity <Bryant\_CSMSlice> in library <work> (architecture <behv>) with generics.

W = 40

Analyzing hierarchy for entity <Bryant\_CSMSlice> in library <work> (architecture <behv>) with generics.

W = 41

Analyzing hierarchy for entity <Bryant\_CSMSlice> in library <work> (architecture <behv>) with generics.

W = 42

Analyzing hierarchy for entity <Bryant\_CSMSlice> in library <work> (architecture <behv>) with generics.

W = 43

Analyzing hierarchy for entity <Bryant\_CSMSlice> in library <work> (architecture <behv>) with generics.

W = 44

Analyzing hierarchy for entity <Bryant\_CSMSlice> in library <work> (architecture <behv>) with generics.

W = 45

Analyzing hierarchy for entity <Bryant\_CSMSlice> in library <work> (architecture <behv>) with generics.

W = 46

Analyzing hierarchy for entity <Bryant\_CSMLastSlice> in library <work> (architecture <behv>) with generics.

W = 47

=========================================================================

\* HDL Analysis \*

=========================================================================

Analyzing generic Entity <Bryant\_CSM\_8B> in library <work> (Architecture <CSM\_8B>).

BITS2 = 2

BITS4 = 4

BITS6 = 6

BITS8 = 8

W = 24

Entity <Bryant\_CSM\_8B> analyzed. Unit <Bryant\_CSM\_8B> generated.

Analyzing generic Entity <Bryant\_CSMSlice\_8B.1> in library <work> (Architecture <behv>).

BBITS = 8

W = 24

Entity <Bryant\_CSMSlice\_8B.1> analyzed. Unit <Bryant\_CSMSlice\_8B.1> generated.

Analyzing generic Entity <Bryant\_CSMSlice.1> in library <work> (Architecture <behv>).

W = 24

Entity <Bryant\_CSMSlice.1> analyzed. Unit <Bryant\_CSMSlice.1> generated.

Analyzing generic Entity <Bryant\_CSMSlice.2> in library <work> (Architecture <behv>).

W = 25

Entity <Bryant\_CSMSlice.2> analyzed. Unit <Bryant\_CSMSlice.2> generated.

Analyzing generic Entity <Bryant\_CSMSlice.3> in library <work> (Architecture <behv>).

W = 26

Entity <Bryant\_CSMSlice.3> analyzed. Unit <Bryant\_CSMSlice.3> generated.

Analyzing generic Entity <Bryant\_CSMSlice.4> in library <work> (Architecture <behv>).

W = 27

Entity <Bryant\_CSMSlice.4> analyzed. Unit <Bryant\_CSMSlice.4> generated.

Analyzing generic Entity <Bryant\_CSMSlice.5> in library <work> (Architecture <behv>).

W = 28

Entity <Bryant\_CSMSlice.5> analyzed. Unit <Bryant\_CSMSlice.5> generated.

Analyzing generic Entity <Bryant\_CSMSlice.6> in library <work> (Architecture <behv>).

W = 29

Entity <Bryant\_CSMSlice.6> analyzed. Unit <Bryant\_CSMSlice.6> generated.

Analyzing generic Entity <Bryant\_CSMSlice.7> in library <work> (Architecture <behv>).

W = 30

Entity <Bryant\_CSMSlice.7> analyzed. Unit <Bryant\_CSMSlice.7> generated.

Analyzing generic Entity <Bryant\_CSMSlice.8> in library <work> (Architecture <behv>).

W = 31

Entity <Bryant\_CSMSlice.8> analyzed. Unit <Bryant\_CSMSlice.8> generated.

Analyzing generic Entity <Bryant\_GenReg.1> in library <work> (Architecture <reg16bit\_arch>).

bbits = 16

w = 32

Entity <Bryant\_GenReg.1> analyzed. Unit <Bryant\_GenReg.1> generated.

Analyzing generic Entity <Bryant\_CSMSlice\_8B.2> in library <work> (Architecture <behv>).

BBITS = 8

W = 32

Entity <Bryant\_CSMSlice\_8B.2> analyzed. Unit <Bryant\_CSMSlice\_8B.2> generated.

Analyzing generic Entity <Bryant\_CSMSlice.9> in library <work> (Architecture <behv>).

W = 32

Entity <Bryant\_CSMSlice.9> analyzed. Unit <Bryant\_CSMSlice.9> generated.

Analyzing generic Entity <Bryant\_CSMSlice.10> in library <work> (Architecture <behv>).

W = 33

Entity <Bryant\_CSMSlice.10> analyzed. Unit <Bryant\_CSMSlice.10> generated.

Analyzing generic Entity <Bryant\_CSMSlice.11> in library <work> (Architecture <behv>).

W = 34

Entity <Bryant\_CSMSlice.11> analyzed. Unit <Bryant\_CSMSlice.11> generated.

Analyzing generic Entity <Bryant\_CSMSlice.12> in library <work> (Architecture <behv>).

W = 35

Entity <Bryant\_CSMSlice.12> analyzed. Unit <Bryant\_CSMSlice.12> generated.

Analyzing generic Entity <Bryant\_CSMSlice.13> in library <work> (Architecture <behv>).

W = 36

Entity <Bryant\_CSMSlice.13> analyzed. Unit <Bryant\_CSMSlice.13> generated.

Analyzing generic Entity <Bryant\_CSMSlice.14> in library <work> (Architecture <behv>).

W = 37

Entity <Bryant\_CSMSlice.14> analyzed. Unit <Bryant\_CSMSlice.14> generated.

Analyzing generic Entity <Bryant\_CSMSlice.15> in library <work> (Architecture <behv>).

W = 38

Entity <Bryant\_CSMSlice.15> analyzed. Unit <Bryant\_CSMSlice.15> generated.

Analyzing generic Entity <Bryant\_CSMSlice.16> in library <work> (Architecture <behv>).

W = 39

Entity <Bryant\_CSMSlice.16> analyzed. Unit <Bryant\_CSMSlice.16> generated.

Analyzing generic Entity <Bryant\_GenReg.2> in library <work> (Architecture <reg16bit\_arch>).

bbits = 32

w = 40

Entity <Bryant\_GenReg.2> analyzed. Unit <Bryant\_GenReg.2> generated.

Analyzing generic Entity <Bryant\_CSMLastSlice\_8B> in library <work> (Architecture <behv>).

BBITS = 8

W = 40

Entity <Bryant\_CSMLastSlice\_8B> analyzed. Unit <Bryant\_CSMLastSlice\_8B> generated.

Analyzing generic Entity <Bryant\_CSMSlice.17> in library <work> (Architecture <behv>).

W = 40

Entity <Bryant\_CSMSlice.17> analyzed. Unit <Bryant\_CSMSlice.17> generated.

Analyzing generic Entity <Bryant\_CSMSlice.18> in library <work> (Architecture <behv>).

W = 41

Entity <Bryant\_CSMSlice.18> analyzed. Unit <Bryant\_CSMSlice.18> generated.

Analyzing generic Entity <Bryant\_CSMSlice.19> in library <work> (Architecture <behv>).

W = 42

Entity <Bryant\_CSMSlice.19> analyzed. Unit <Bryant\_CSMSlice.19> generated.

Analyzing generic Entity <Bryant\_CSMSlice.20> in library <work> (Architecture <behv>).

W = 43

Entity <Bryant\_CSMSlice.20> analyzed. Unit <Bryant\_CSMSlice.20> generated.

Analyzing generic Entity <Bryant\_CSMSlice.21> in library <work> (Architecture <behv>).

W = 44

Entity <Bryant\_CSMSlice.21> analyzed. Unit <Bryant\_CSMSlice.21> generated.

Analyzing generic Entity <Bryant\_CSMSlice.22> in library <work> (Architecture <behv>).

W = 45

Entity <Bryant\_CSMSlice.22> analyzed. Unit <Bryant\_CSMSlice.22> generated.

Analyzing generic Entity <Bryant\_CSMSlice.23> in library <work> (Architecture <behv>).

W = 46

Entity <Bryant\_CSMSlice.23> analyzed. Unit <Bryant\_CSMSlice.23> generated.

Analyzing generic Entity <Bryant\_CSMLastSlice> in library <work> (Architecture <behv>).

W = 47

Entity <Bryant\_CSMLastSlice> analyzed. Unit <Bryant\_CSMLastSlice> generated.

Analyzing generic Entity <Bryant\_GenRegLast> in library <work> (Architecture <reg16bit\_arch>).

w = 48

Entity <Bryant\_GenRegLast> analyzed. Unit <Bryant\_GenRegLast> generated.

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\* HDL Synthesis \*

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Performing bidirectional port resolution...

Synthesizing Unit <Bryant\_GenReg\_1>.

Related source file is "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

Found 32-bit register for signal <sAout>.

Found 16-bit register for signal <sBout>.

Found 32-bit register for signal <scarryout>.

Found 32-bit register for signal <sSumout>.

Summary:

inferred 112 D-type flip-flop(s).

Unit <Bryant\_GenReg\_1> synthesized.

Synthesizing Unit <Bryant\_GenReg\_2>.

Related source file is "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

Found 40-bit register for signal <sAout>.

Found 8-bit register for signal <sBout>.

Found 40-bit register for signal <scarryout>.

Found 40-bit register for signal <sSumout>.

Summary:

inferred 128 D-type flip-flop(s).

Unit <Bryant\_GenReg\_2> synthesized.

Synthesizing Unit <Bryant\_GenRegLast>.

Related source file is "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

Found 48-bit register for signal <scarryout>.

Found 48-bit register for signal <sSumout>.

Summary:

inferred 96 D-type flip-flop(s).

Unit <Bryant\_GenRegLast> synthesized.

Synthesizing Unit <Bryant\_CSMSlice\_1>.

Related source file is "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

Found 24-bit xor3 for signal <SumOut<23:0>>.

Summary:

inferred 24 Xor(s).

Unit <Bryant\_CSMSlice\_1> synthesized.

Synthesizing Unit <Bryant\_CSMSlice\_2>.

Related source file is "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

Found 25-bit xor3 for signal <SumOut<24:0>>.

Summary:

inferred 25 Xor(s).

Unit <Bryant\_CSMSlice\_2> synthesized.

Synthesizing Unit <Bryant\_CSMSlice\_3>.

Related source file is "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

Found 26-bit xor3 for signal <SumOut<25:0>>.

Summary:

inferred 26 Xor(s).

Unit <Bryant\_CSMSlice\_3> synthesized.

Synthesizing Unit <Bryant\_CSMSlice\_4>.

Related source file is "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

Found 27-bit xor3 for signal <SumOut<26:0>>.

Summary:

inferred 27 Xor(s).

Unit <Bryant\_CSMSlice\_4> synthesized.

Synthesizing Unit <Bryant\_CSMSlice\_5>.

Related source file is "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

Found 28-bit xor3 for signal <SumOut<27:0>>.

Summary:

inferred 28 Xor(s).

Unit <Bryant\_CSMSlice\_5> synthesized.

Synthesizing Unit <Bryant\_CSMSlice\_6>.

Related source file is "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

Found 29-bit xor3 for signal <SumOut<28:0>>.

Summary:

inferred 29 Xor(s).

Unit <Bryant\_CSMSlice\_6> synthesized.

Synthesizing Unit <Bryant\_CSMSlice\_7>.

Related source file is "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

Found 30-bit xor3 for signal <SumOut<29:0>>.

Summary:

inferred 30 Xor(s).

Unit <Bryant\_CSMSlice\_7> synthesized.

Synthesizing Unit <Bryant\_CSMSlice\_8>.

Related source file is "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

Found 31-bit xor3 for signal <SumOut<30:0>>.

Summary:

inferred 31 Xor(s).

Unit <Bryant\_CSMSlice\_8> synthesized.

Synthesizing Unit <Bryant\_CSMSlice\_9>.

Related source file is "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

Found 32-bit xor3 for signal <SumOut<31:0>>.

Summary:

inferred 32 Xor(s).

Unit <Bryant\_CSMSlice\_9> synthesized.

Synthesizing Unit <Bryant\_CSMSlice\_10>.

Related source file is "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

Found 33-bit xor3 for signal <SumOut<32:0>>.

Summary:

inferred 33 Xor(s).

Unit <Bryant\_CSMSlice\_10> synthesized.

Synthesizing Unit <Bryant\_CSMSlice\_11>.

Related source file is "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

Found 34-bit xor3 for signal <SumOut<33:0>>.

Summary:

inferred 34 Xor(s).

Unit <Bryant\_CSMSlice\_11> synthesized.

Synthesizing Unit <Bryant\_CSMSlice\_12>.

Related source file is "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

Found 35-bit xor3 for signal <SumOut<34:0>>.

Summary:

inferred 35 Xor(s).

Unit <Bryant\_CSMSlice\_12> synthesized.

Synthesizing Unit <Bryant\_CSMSlice\_13>.

Related source file is "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

Found 36-bit xor3 for signal <SumOut<35:0>>.

Summary:

inferred 36 Xor(s).

Unit <Bryant\_CSMSlice\_13> synthesized.

Synthesizing Unit <Bryant\_CSMSlice\_14>.

Related source file is "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

Found 37-bit xor3 for signal <SumOut<36:0>>.

Summary:

inferred 37 Xor(s).

Unit <Bryant\_CSMSlice\_14> synthesized.

Synthesizing Unit <Bryant\_CSMSlice\_15>.

Related source file is "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

Found 38-bit xor3 for signal <SumOut<37:0>>.

Summary:

inferred 38 Xor(s).

Unit <Bryant\_CSMSlice\_15> synthesized.

Synthesizing Unit <Bryant\_CSMSlice\_16>.

Related source file is "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

Found 39-bit xor3 for signal <SumOut<38:0>>.

Summary:

inferred 39 Xor(s).

Unit <Bryant\_CSMSlice\_16> synthesized.

Synthesizing Unit <Bryant\_CSMSlice\_17>.

Related source file is "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

Found 40-bit xor3 for signal <SumOut<39:0>>.

Summary:

inferred 40 Xor(s).

Unit <Bryant\_CSMSlice\_17> synthesized.

Synthesizing Unit <Bryant\_CSMSlice\_18>.

Related source file is "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

Found 41-bit xor3 for signal <SumOut<40:0>>.

Summary:

inferred 41 Xor(s).

Unit <Bryant\_CSMSlice\_18> synthesized.

Synthesizing Unit <Bryant\_CSMSlice\_19>.

Related source file is "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

Found 42-bit xor3 for signal <SumOut<41:0>>.

Summary:

inferred 42 Xor(s).

Unit <Bryant\_CSMSlice\_19> synthesized.

Synthesizing Unit <Bryant\_CSMSlice\_20>.

Related source file is "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

Found 43-bit xor3 for signal <SumOut<42:0>>.

Summary:

inferred 43 Xor(s).

Unit <Bryant\_CSMSlice\_20> synthesized.

Synthesizing Unit <Bryant\_CSMSlice\_21>.

Related source file is "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

Found 44-bit xor3 for signal <SumOut<43:0>>.

Summary:

inferred 44 Xor(s).

Unit <Bryant\_CSMSlice\_21> synthesized.

Synthesizing Unit <Bryant\_CSMSlice\_22>.

Related source file is "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

Found 45-bit xor3 for signal <SumOut<44:0>>.

Summary:

inferred 45 Xor(s).

Unit <Bryant\_CSMSlice\_22> synthesized.

Synthesizing Unit <Bryant\_CSMSlice\_23>.

Related source file is "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

Found 46-bit xor3 for signal <SumOut<45:0>>.

Summary:

inferred 46 Xor(s).

Unit <Bryant\_CSMSlice\_23> synthesized.

Synthesizing Unit <Bryant\_CSMLastSlice>.

Related source file is "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

Found 47-bit xor3 for signal <SumOut<46:0>>.

Summary:

inferred 47 Xor(s).

Unit <Bryant\_CSMLastSlice> synthesized.

Synthesizing Unit <Bryant\_CSMSlice\_8B\_1>.

Related source file is "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

Unit <Bryant\_CSMSlice\_8B\_1> synthesized.

Synthesizing Unit <Bryant\_CSMSlice\_8B\_2>.

Related source file is "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

Unit <Bryant\_CSMSlice\_8B\_2> synthesized.

Synthesizing Unit <Bryant\_CSMLastSlice\_8B>.

Related source file is "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Bryant\_CSM\_Components.vhdl".

Unit <Bryant\_CSMLastSlice\_8B> synthesized.

Synthesizing Unit <Bryant\_CSM\_8B>.

Related source file is "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSM\_8B.vhdl".

WARNING:Xst:653 - Signal <sSumOut0> is used but never assigned. This sourceless signal will be automatically connected to value 000000000000000000000000.

WARNING:Xst:653 - Signal <sCarryIn> is used but never assigned. This sourceless signal will be automatically connected to value 000000000000000000000000.

Found 48-bit adder for signal <SumOut>.

Summary:

inferred 1 Adder/Subtractor(s).

Unit <Bryant\_CSM\_8B> synthesized.

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HDL Synthesis Report

Macro Statistics

# Adders/Subtractors : 1

48-bit adder : 1

# Registers : 10

16-bit register : 1

32-bit register : 3

40-bit register : 3

48-bit register : 2

8-bit register : 1

# Xors : 852

1-bit xor3 : 852

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\* Advanced HDL Synthesis \*

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WARNING:Xst:1710 - FF/Latch <scarryout\_4> (without init value) has a constant value of 0 in block <InstBryant\_GenReg3>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_3> (without init value) has a constant value of 0 in block <InstBryant\_GenReg3>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_2> (without init value) has a constant value of 0 in block <InstBryant\_GenReg3>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_1> (without init value) has a constant value of 0 in block <InstBryant\_GenReg3>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_0> (without init value) has a constant value of 0 in block <InstBryant\_GenReg3>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <sSumout\_47> (without init value) has a constant value of 0 in block <InstBryant\_GenReg3>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_39> (without init value) has a constant value of 0 in block <InstBryant\_GenReg2>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_15> (without init value) has a constant value of 0 in block <InstBryant\_GenReg2>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_14> (without init value) has a constant value of 0 in block <InstBryant\_GenReg2>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_13> (without init value) has a constant value of 0 in block <InstBryant\_GenReg2>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_12> (without init value) has a constant value of 0 in block <InstBryant\_GenReg2>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_11> (without init value) has a constant value of 0 in block <InstBryant\_GenReg2>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_10> (without init value) has a constant value of 0 in block <InstBryant\_GenReg2>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_9> (without init value) has a constant value of 0 in block <InstBryant\_GenReg2>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_8> (without init value) has a constant value of 0 in block <InstBryant\_GenReg2>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_7> (without init value) has a constant value of 0 in block <InstBryant\_GenReg2>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_6> (without init value) has a constant value of 0 in block <InstBryant\_GenReg2>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_5> (without init value) has a constant value of 0 in block <InstBryant\_GenReg2>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_4> (without init value) has a constant value of 0 in block <InstBryant\_GenReg2>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_47> (without init value) has a constant value of 0 in block <InstBryant\_GenReg3>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_23> (without init value) has a constant value of 0 in block <InstBryant\_GenReg3>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_22> (without init value) has a constant value of 0 in block <InstBryant\_GenReg3>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_21> (without init value) has a constant value of 0 in block <InstBryant\_GenReg3>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_20> (without init value) has a constant value of 0 in block <InstBryant\_GenReg3>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_19> (without init value) has a constant value of 0 in block <InstBryant\_GenReg3>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_18> (without init value) has a constant value of 0 in block <InstBryant\_GenReg3>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_17> (without init value) has a constant value of 0 in block <InstBryant\_GenReg3>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_16> (without init value) has a constant value of 0 in block <InstBryant\_GenReg3>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_15> (without init value) has a constant value of 0 in block <InstBryant\_GenReg3>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_14> (without init value) has a constant value of 0 in block <InstBryant\_GenReg3>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_13> (without init value) has a constant value of 0 in block <InstBryant\_GenReg3>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_12> (without init value) has a constant value of 0 in block <InstBryant\_GenReg3>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_11> (without init value) has a constant value of 0 in block <InstBryant\_GenReg3>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_10> (without init value) has a constant value of 0 in block <InstBryant\_GenReg3>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_9> (without init value) has a constant value of 0 in block <InstBryant\_GenReg3>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_8> (without init value) has a constant value of 0 in block <InstBryant\_GenReg3>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_7> (without init value) has a constant value of 0 in block <InstBryant\_GenReg3>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_6> (without init value) has a constant value of 0 in block <InstBryant\_GenReg3>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_5> (without init value) has a constant value of 0 in block <InstBryant\_GenReg3>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <sAout\_0> (without init value) has a constant value of 0 in block <InstBryant\_GenReg2>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_31> (without init value) has a constant value of 0 in block <InstBryant\_GenReg1>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_7> (without init value) has a constant value of 0 in block <InstBryant\_GenReg1>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_6> (without init value) has a constant value of 0 in block <InstBryant\_GenReg1>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_5> (without init value) has a constant value of 0 in block <InstBryant\_GenReg1>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_4> (without init value) has a constant value of 0 in block <InstBryant\_GenReg1>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_3> (without init value) has a constant value of 0 in block <InstBryant\_GenReg1>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_2> (without init value) has a constant value of 0 in block <InstBryant\_GenReg1>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_1> (without init value) has a constant value of 0 in block <InstBryant\_GenReg1>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_0> (without init value) has a constant value of 0 in block <InstBryant\_GenReg1>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <sSumout\_31> (without init value) has a constant value of 0 in block <InstBryant\_GenReg1>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <sAout\_7> (without init value) has a constant value of 0 in block <InstBryant\_GenReg1>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <sAout\_6> (without init value) has a constant value of 0 in block <InstBryant\_GenReg1>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <sAout\_5> (without init value) has a constant value of 0 in block <InstBryant\_GenReg1>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <sAout\_4> (without init value) has a constant value of 0 in block <InstBryant\_GenReg1>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <sAout\_3> (without init value) has a constant value of 0 in block <InstBryant\_GenReg1>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <sAout\_2> (without init value) has a constant value of 0 in block <InstBryant\_GenReg1>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <sAout\_1> (without init value) has a constant value of 0 in block <InstBryant\_GenReg1>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <sAout\_0> (without init value) has a constant value of 0 in block <InstBryant\_GenReg1>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_3> (without init value) has a constant value of 0 in block <InstBryant\_GenReg2>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_2> (without init value) has a constant value of 0 in block <InstBryant\_GenReg2>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_1> (without init value) has a constant value of 0 in block <InstBryant\_GenReg2>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <scarryout\_0> (without init value) has a constant value of 0 in block <InstBryant\_GenReg2>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <sSumout\_39> (without init value) has a constant value of 0 in block <InstBryant\_GenReg2>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <sAout\_15> (without init value) has a constant value of 0 in block <InstBryant\_GenReg2>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <sAout\_14> (without init value) has a constant value of 0 in block <InstBryant\_GenReg2>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <sAout\_13> (without init value) has a constant value of 0 in block <InstBryant\_GenReg2>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <sAout\_12> (without init value) has a constant value of 0 in block <InstBryant\_GenReg2>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <sAout\_11> (without init value) has a constant value of 0 in block <InstBryant\_GenReg2>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <sAout\_10> (without init value) has a constant value of 0 in block <InstBryant\_GenReg2>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <sAout\_9> (without init value) has a constant value of 0 in block <InstBryant\_GenReg2>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <sAout\_8> (without init value) has a constant value of 0 in block <InstBryant\_GenReg2>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <sAout\_7> (without init value) has a constant value of 0 in block <InstBryant\_GenReg2>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <sAout\_6> (without init value) has a constant value of 0 in block <InstBryant\_GenReg2>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <sAout\_5> (without init value) has a constant value of 0 in block <InstBryant\_GenReg2>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <sAout\_4> (without init value) has a constant value of 0 in block <InstBryant\_GenReg2>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <sAout\_3> (without init value) has a constant value of 0 in block <InstBryant\_GenReg2>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <sAout\_2> (without init value) has a constant value of 0 in block <InstBryant\_GenReg2>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <sAout\_1> (without init value) has a constant value of 0 in block <InstBryant\_GenReg2>. This FF/Latch will be trimmed during the optimization process.

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Advanced HDL Synthesis Report

Macro Statistics

# Adders/Subtractors : 1

48-bit adder : 1

# Registers : 336

Flip-Flops : 336

# Xors : 852

1-bit xor3 : 852

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\* Low Level Synthesis \*

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Optimizing unit <Bryant\_CSM\_8B> ...

Optimizing unit <Bryant\_GenReg\_1> ...

Optimizing unit <Bryant\_GenReg\_2> ...

Optimizing unit <Bryant\_GenRegLast> ...

Optimizing unit <Bryant\_CSMSlice\_8> ...

Optimizing unit <Bryant\_CSMSlice\_9> ...

Optimizing unit <Bryant\_CSMSlice\_10> ...

Optimizing unit <Bryant\_CSMSlice\_11> ...

Optimizing unit <Bryant\_CSMSlice\_12> ...

Optimizing unit <Bryant\_CSMSlice\_13> ...

Optimizing unit <Bryant\_CSMSlice\_14> ...

Optimizing unit <Bryant\_CSMSlice\_15> ...

Optimizing unit <Bryant\_CSMSlice\_16> ...

Optimizing unit <Bryant\_CSMSlice\_17> ...

Optimizing unit <Bryant\_CSMSlice\_18> ...

Optimizing unit <Bryant\_CSMSlice\_19> ...

Optimizing unit <Bryant\_CSMSlice\_20> ...

Optimizing unit <Bryant\_CSMSlice\_21> ...

Optimizing unit <Bryant\_CSMSlice\_22> ...

Optimizing unit <Bryant\_CSMSlice\_23> ...

Optimizing unit <Bryant\_CSMLastSlice> ...

Optimizing unit <Bryant\_CSMSlice\_8B\_1> ...

Optimizing unit <Bryant\_CSMSlice\_8B\_2> ...

Optimizing unit <Bryant\_CSMLastSlice\_8B> ...

WARNING:Xst:1710 - FF/Latch <InstBryant\_GenReg3/scarryout\_17> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg3/scarryout\_18> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg3/scarryout\_19> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg3/scarryout\_20> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg3/scarryout\_21> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg3/scarryout\_22> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg3/scarryout\_23> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg3/scarryout\_47> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg2/sAout\_0> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg2/sAout\_1> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg2/sAout\_2> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg2/sAout\_3> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg2/sAout\_4> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg2/sAout\_5> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg2/sAout\_6> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg2/sAout\_7> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg2/sSumout\_39> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg3/sSumout\_47> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg3/scarryout\_0> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg3/scarryout\_1> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg3/scarryout\_2> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg3/scarryout\_3> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg3/scarryout\_4> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg3/scarryout\_5> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg3/scarryout\_6> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg3/scarryout\_7> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg3/scarryout\_8> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg3/scarryout\_9> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg3/scarryout\_10> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg3/scarryout\_11> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg3/scarryout\_12> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg3/scarryout\_13> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg3/scarryout\_14> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg3/scarryout\_15> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg3/scarryout\_16> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg2/scarryout\_14> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg2/scarryout\_15> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg2/scarryout\_39> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg1/sAout\_0> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg1/sAout\_1> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg1/sAout\_2> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg1/sAout\_3> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg1/sAout\_4> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg1/sAout\_5> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg1/sAout\_6> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg1/sAout\_7> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg1/sSumout\_31> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg1/scarryout\_0> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg1/scarryout\_1> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg1/scarryout\_2> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg1/scarryout\_3> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg1/scarryout\_4> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg1/scarryout\_5> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg1/scarryout\_6> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg1/scarryout\_7> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg1/scarryout\_31> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg2/scarryout\_0> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg2/scarryout\_1> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg2/scarryout\_2> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg2/scarryout\_3> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg2/scarryout\_4> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg2/scarryout\_5> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg2/scarryout\_6> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg2/scarryout\_7> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg2/scarryout\_8> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg2/scarryout\_9> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg2/scarryout\_10> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg2/scarryout\_11> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg2/scarryout\_12> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg2/scarryout\_13> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg2/sAout\_8> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg2/sAout\_9> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg2/sAout\_10> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg2/sAout\_11> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg2/sAout\_12> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg2/sAout\_13> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg2/sAout\_14> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <InstBryant\_GenReg2/sAout\_15> (without init value) has a constant value of 0 in block <Bryant\_CSM\_8B>. This FF/Latch will be trimmed during the optimization process.

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block Bryant\_CSM\_8B, actual ratio is 1.

FlipFlop InstBryant\_GenReg1/sBout\_0 has been replicated 2 time(s)

INFO:Xst:1843 - HDL ADVISOR - FlipFlop InstBryant\_GenReg1/sBout\_0 connected to a primary input has been replicated

FlipFlop InstBryant\_GenReg2/sBout\_0 has been replicated 2 time(s)

Final Macro Processing ...

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Final Register Report

Macro Statistics

# Registers : 262

Flip-Flops : 262

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\* Partition Report \*

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Partition Implementation Status

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No Partitions were found in this design.

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=========================================================================

\* Final Report \*

=========================================================================

Final Results

RTL Top Level Output File Name : Bryant\_CSM\_8B.ngr

Top Level Output File Name : Bryant\_CSM\_8B

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : No

Design Statistics

# IOs : 99

Cell Usage :

# BELS : 1305

# GND : 1

# LUT1 : 24

# LUT2 : 41

# LUT2\_D : 2

# LUT2\_L : 2

# LUT3 : 12

# LUT3\_D : 4

# LUT4 : 783

# LUT4\_D : 315

# LUT4\_L : 10

# MUXCY : 47

# MUXF5 : 16

# XORCY : 48

# FlipFlops/Latches : 262

# FDRE : 262

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 98

# IBUF : 50

# OBUF : 48

=========================================================================

Device utilization summary:

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Selected Device : 4vlx100ff1148-12

Number of Slices: 631 out of 49152 1%

Number of Slice Flip Flops: 262 out of 98304 0%

Number of 4 input LUTs: 1193 out of 98304 1%

Number of IOs: 99

Number of bonded IOBs: 99 out of 768 12%

Number of GCLKs: 1 out of 32 3%

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Partition Resource Summary:

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No Partitions were found in this design.

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TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

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-----------------------------------+------------------------+-------+

Clock Signal | Clock buffer(FF name) | Load |

-----------------------------------+------------------------+-------+

clk | BUFGP | 262 |

-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:

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No asynchronous control signals found in this design

Timing Summary:

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Speed Grade: -12

Minimum period: 5.298ns (Maximum Frequency: 188.749MHz)

Minimum input arrival time before clock: 6.218ns

Maximum output required time after clock: 6.443ns

Maximum combinational path delay: No path found

Timing Detail:

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All values displayed in nanoseconds (ns)

=========================================================================

Timing constraint: Default period analysis for Clock 'clk'

Clock period: 5.298ns (frequency: 188.749MHz)

Total number of paths / destination ports: 65216 / 166

-------------------------------------------------------------------------

Delay: 5.298ns (Levels of Logic = 8)

Source: InstBryant\_GenReg1/sAout\_29 (FF)

Destination: InstBryant\_GenReg2/sSumout\_31 (FF)

Source Clock: clk rising

Destination Clock: clk rising

Data Path: InstBryant\_GenReg1/sAout\_29 to InstBryant\_GenReg2/sSumout\_31

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FDRE:C->Q 26 0.272 0.838 InstBryant\_GenReg1/sAout\_29 (InstBryant\_GenReg1/sAout\_29)

LUT4\_D:I2->O 1 0.147 0.436 InstBryant\_CSMSlice\_8B2/InstBryant\_CSMSlice1/Mxor\_SumOut<29>\_xo<0>1 (InstBryant\_CSMSlice\_8B2/s1<29>)

LUT4\_D:I2->O 1 0.147 0.388 InstBryant\_CSMSlice\_8B2/InstBryant\_CSMSlice2/CarryOut\_30\_or00001 (InstBryant\_CSMSlice\_8B2/c2<30>)

LUT4:I3->O 2 0.147 0.449 InstBryant\_CSMSlice\_8B2/InstBryant\_CSMSlice3/Mxor\_SumOut<30>\_xo<0>1 (InstBryant\_CSMSlice\_8B2/s3<30>)

LUT4\_D:I2->O 1 0.147 0.436 InstBryant\_CSMSlice\_8B2/InstBryant\_CSMSlice4/Mxor\_SumOut<30>\_xo<0>1 (InstBryant\_CSMSlice\_8B2/s4<30>)

LUT4:I2->O 2 0.147 0.401 InstBryant\_CSMSlice\_8B2/InstBryant\_CSMSlice5/CarryOut\_31\_or00001 (InstBryant\_CSMSlice\_8B2/c5<31>)

LUT4:I3->O 2 0.147 0.449 InstBryant\_CSMSlice\_8B2/InstBryant\_CSMSlice6/Mxor\_SumOut<31>\_xo<0>1 (InstBryant\_CSMSlice\_8B2/s6<31>)

LUT4\_D:I2->O 1 0.147 0.436 InstBryant\_CSMSlice\_8B2/InstBryant\_CSMSlice7/Mxor\_SumOut<31>\_xo<0>1 (InstBryant\_CSMSlice\_8B2/s7<31>)

LUT4:I2->O 1 0.147 0.000 InstBryant\_CSMSlice\_8B2/InstBryant\_CSMSlice8/Mxor\_SumOut<31>\_xo<0>1 (sSumOut2<31>)

FDRE:D 0.017 InstBryant\_GenReg2/sSumout\_31

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Total 5.298ns (1.465ns logic, 3.833ns route)

(27.7% logic, 72.3% route)

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Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'

Total number of paths / destination ports: 16708 / 620

-------------------------------------------------------------------------

Offset: 6.218ns (Levels of Logic = 8)

Source: InB<0> (PAD)

Destination: InstBryant\_GenReg1/scarryout\_30 (FF)

Destination Clock: clk rising

Data Path: InB<0> to InstBryant\_GenReg1/scarryout\_30

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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IBUF:I->O 47 0.754 1.017 InB\_0\_IBUF (InB\_0\_IBUF)

LUT4:I0->O 2 0.147 0.567 InstBryant\_CSMSlice\_8B1/InstBryant\_CSMSlice2/CarryOut\_9\_or00001 (InstBryant\_CSMSlice\_8B1/c2<9>)

LUT4:I0->O 2 0.147 0.567 InstBryant\_CSMSlice\_8B1/InstBryant\_CSMSlice3/CarryOut\_10\_or00001 (InstBryant\_CSMSlice\_8B1/c3<10>)

LUT4:I0->O 2 0.147 0.567 InstBryant\_CSMSlice\_8B1/InstBryant\_CSMSlice4/CarryOut\_11\_or00001 (InstBryant\_CSMSlice\_8B1/c4<11>)

LUT4:I0->O 2 0.147 0.567 InstBryant\_CSMSlice\_8B1/InstBryant\_CSMSlice5/CarryOut\_12\_or00001 (InstBryant\_CSMSlice\_8B1/c5<12>)

LUT4:I0->O 2 0.147 0.567 InstBryant\_CSMSlice\_8B1/InstBryant\_CSMSlice6/CarryOut\_13\_or00001 (InstBryant\_CSMSlice\_8B1/c6<13>)

LUT4:I0->O 2 0.147 0.567 InstBryant\_CSMSlice\_8B1/InstBryant\_CSMSlice7/CarryOut\_14\_or00001 (InstBryant\_CSMSlice\_8B1/c7<14>)

LUT4:I0->O 1 0.147 0.000 InstBryant\_CSMSlice\_8B1/InstBryant\_CSMSlice8/CarryOut\_15\_or00001 (sCarryOut1<15>)

FDRE:D 0.017 InstBryant\_GenReg1/scarryout\_15

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Total 6.218ns (1.800ns logic, 4.418ns route)

(28.9% logic, 71.1% route)

=========================================================================

Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'

Total number of paths / destination ports: 1750 / 48

-------------------------------------------------------------------------

Offset: 6.443ns (Levels of Logic = 50)

Source: InstBryant\_GenReg3/sSumout\_0 (FF)

Destination: SumOut<47> (PAD)

Source Clock: clk rising

Data Path: InstBryant\_GenReg3/sSumout\_0 to SumOut<47>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FDRE:C->Q 1 0.272 0.388 InstBryant\_GenReg3/sSumout\_0 (InstBryant\_GenReg3/sSumout\_0)

LUT1:I0->O 1 0.147 0.000 Madd\_SumOut\_cy<0>\_rt (Madd\_SumOut\_cy<0>\_rt)

MUXCY:S->O 1 0.278 0.000 Madd\_SumOut\_cy<0> (Madd\_SumOut\_cy<0>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<1> (Madd\_SumOut\_cy<1>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<2> (Madd\_SumOut\_cy<2>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<3> (Madd\_SumOut\_cy<3>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<4> (Madd\_SumOut\_cy<4>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<5> (Madd\_SumOut\_cy<5>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<6> (Madd\_SumOut\_cy<6>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<7> (Madd\_SumOut\_cy<7>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<8> (Madd\_SumOut\_cy<8>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<9> (Madd\_SumOut\_cy<9>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<10> (Madd\_SumOut\_cy<10>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<11> (Madd\_SumOut\_cy<11>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<12> (Madd\_SumOut\_cy<12>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<13> (Madd\_SumOut\_cy<13>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<14> (Madd\_SumOut\_cy<14>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<15> (Madd\_SumOut\_cy<15>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<16> (Madd\_SumOut\_cy<16>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<17> (Madd\_SumOut\_cy<17>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<18> (Madd\_SumOut\_cy<18>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<19> (Madd\_SumOut\_cy<19>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<20> (Madd\_SumOut\_cy<20>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<21> (Madd\_SumOut\_cy<21>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<22> (Madd\_SumOut\_cy<22>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<23> (Madd\_SumOut\_cy<23>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<24> (Madd\_SumOut\_cy<24>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<25> (Madd\_SumOut\_cy<25>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<26> (Madd\_SumOut\_cy<26>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<27> (Madd\_SumOut\_cy<27>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<28> (Madd\_SumOut\_cy<28>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<29> (Madd\_SumOut\_cy<29>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<30> (Madd\_SumOut\_cy<30>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<31> (Madd\_SumOut\_cy<31>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<32> (Madd\_SumOut\_cy<32>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<33> (Madd\_SumOut\_cy<33>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<34> (Madd\_SumOut\_cy<34>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<35> (Madd\_SumOut\_cy<35>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<36> (Madd\_SumOut\_cy<36>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<37> (Madd\_SumOut\_cy<37>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<38> (Madd\_SumOut\_cy<38>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<39> (Madd\_SumOut\_cy<39>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<40> (Madd\_SumOut\_cy<40>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<41> (Madd\_SumOut\_cy<41>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<42> (Madd\_SumOut\_cy<42>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<43> (Madd\_SumOut\_cy<43>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<44> (Madd\_SumOut\_cy<44>)

MUXCY:CI->O 1 0.034 0.000 Madd\_SumOut\_cy<45> (Madd\_SumOut\_cy<45>)

MUXCY:CI->O 0 0.034 0.000 Madd\_SumOut\_cy<46> (Madd\_SumOut\_cy<46>)

XORCY:CI->O 1 0.273 0.266 Madd\_SumOut\_xor<47> (SumOut\_47\_OBUF)

OBUF:I->O 3.255 SumOut\_47\_OBUF (SumOut<47>)

----------------------------------------

Total 6.443ns (5.789ns logic, 0.654ns route)

(89.8% logic, 10.2% route)

=========================================================================

Total REAL time to Xst completion: 15.00 secs

Total CPU time to Xst completion: 14.61 secs

-->

Total memory usage is 4605940 kilobytes

Number of errors : 0 ( 0 filtered)

Number of warnings : 182 ( 0 filtered)

Number of infos : 1 ( 0 filtered)